UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,216	06/25/2001	Joseph I. Chamdani	PA1749US	1441

5073 7590 09/29/2005

BAKER BOTTS L.L.P.
2001 ROSS AVENUE
SUITE 600
DALLAS, TX 75201-2980

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,216	CHAMDANI ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54,57-63,67,68,71-77,79 and 80* is/are rejected.

7)☒ Claim(s) *55,56,64-66,69,70 and 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract discloses a legal phraseology "**comprises**" in lines 1 and 4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

> The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

Claim Objections

2. Claim 13, 15,48,49, 51 and 66 are objected to because of the following informalities:

Claim 13 recites, "GBIC" in line 2. It is suggested to describe the acronym when reciting for the first time in the claim.

Claim 15 recites, "**a** packet" in line 3 and "**a** packet" in line 6. For clarity, it is suggested to change the "a packet" in line 6 to "**the** packet".

Claim 48 recites, "RAID" in line 2. It is suggested to describe the acronym when reciting for the first time in the claim.

Claim 49 recites, "JBOD" in line 2. It is suggested to describe the acronym when reciting for the first time in the claim.

Claim 51 recites, "**a** packet" in line 1 and "a packet" in line 2. For clarity, it is suggested to change the "a packet" in line 2 to "**the** packet".

Claim 66 recites, "FLC" in line 2. It is suggested to describe the acronym when reciting for the first time in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1,15,25,35,51-54,57,58,71,73, and 74 are rejected under 35 U.S.C. 102(e) as being anticipated by Zadikian (US006724757B1).

Regarding Claim 1, Zadikian discloses a switching device (see FIG. 1, Router 100; or also see FIG. 3, Router 300 and FIG. 4, Router 400) comprising:

at least two base racks (see FIG. 4, multi-shelves/racks within a bay 400; also see FIG. 3; group 310 (1-N); see col. 8, line 10; col. 12, line 44-59), each base rack including a line card (see FIG. 4, line cards, LC 410; also see FIG. 3, line cards 220 (1,1)...(1, N)...(N,N)) having at least one port capable of receiving and transmitting a packet (see FIG. 2, Line Card 220; see FIG. 5, Optical Receiver 506 and transmitter 511 port; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH);

a switch card (see FIG. 4, Group Matrices SM 420 (1)-(N); also see FIG. 3, Group Matrix 212 (1-N) an 216 (1-N); see col. 9, line 26-41; see col. 12, line 46-67) in communication with the line card across a backplane (see FIG. 4, backplane; see col. 13, line 19-26);

the at least two base racks coupled such that the switch cards from of each base rack are in communication (see FIG. 4, SM 420 from the first shelf to SM 420 in the second shelf; also see FIG. 3, Group Matrix 212 (1) from group 310 (1) is in communication with Group Matrix 212 (N) from group 321 (1); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44).

Regarding Claim 15, Zadikian discloses a switching device (see FIG. 1, Router 100; or also see FIG. 3, Router 300 and FIG. 4, Router 400) comprising:

a first base rack (see FIG. 4, a first shelf within a bay 400; also see FIG. 3; group 310 (1); see col. 8, line 10; col. 12, line 44-59) including a first line card (see FIG. 4, line card, LC 410 in the first shelf; also see.FIG. 3, line card 220 (1,1)) having a first port capable of receiving a packet (see FIG. 2, a port in Line Card 220; also see FIG. 5, Optical Receiver 506 and transmitter 511 port; see col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH);

a first switch card (see FIG. 4, Group Matrix SM 420 (1); also see FIG. 3, Group Matrix 212 (1-N)); see col. 9, line 26-41; see col. 12, line 46-67) in communication with the first line card (see FIG. 4, communicates via backplane; see col. 13, line 19-26);

a second base rack (see FIG. 4, a second shelf within a bay 400; also see FIG. 3; group 310 (N); see col. 8, line 10; col. 12, line 44-59) including a second line card (see FIG. 4, line card, LC 410 in the second shelf; also see FIG. 3, line card 220 (1,N)) having a second port capable of transmitting a packet (see FIG. 2, a port in Line Card 220; also see FIG. 5, Optical Receiver 506 and transmitter 511 port; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH);

a second switch card (see FIG. 4, Group Matrix SM 420 (N); also see FIG. 3, Group Matrix 212 (N)); see col. 9, line 26-41; see col. 12, line 46-67) in communication with the second line card (see FIG. 4, communicates via backplane; see col. 13, line 19-26), and in further communication with the first switch card (see FIG. 4, SM 420 from the first shelf to SM 420 in the second shelf; also see FIG. 3, Group Matrix 212 (1) from group 310 (1) is in communication with Group Matrix 212 (N) from group 321 (1); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44).

Regarding Claim 25, Zadikian discloses a switching device (see FIG. 1, Router 100; or also see FIG. 3, Router 300 and FIG. 4, Router 400) comprising:

a first base rack (see FIG. 4, a first shelf within a bay 400; also see FIG. 3; group 310 (1); see col. 8, line 10; col. 12, line 44-59) including a first line card (see FIG. 4, line card, LC 410 in the first shelf; also see FIG. 3, line card 220 (1,1)) having an ingress port capable of receiving a packet (see FIG. 2, a port in Line Card 220; also see FIG. 5, Optical Receiver 506; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH), the first line card being capable of processing the packet (see FIG. 5, Protocol processor 520, CPU 570, Transceiver 580,transformer 585,switch 590; see col. 13, line 39 to col. 14, line 43);

a first switch card (see FIG. 4, Group Matrix SM 420 (1); also see FIG. 2-3, Group Matrix 212 (1-N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67) in communication with the first line card and capable of accepting the packet therefrom (see FIG. 4, communicates and accepts packets/cells/frames via backplane; see col. 13, line 19-26), the first switch card including a first cascade port (FIG. 2-3, a SM 212 (1) port that interface with

shelf switch or switching matrix), the first switch card capable of routing the packet to the first cascade port (see FIG. 6; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; a group matrix card routes/forwards packets/cells/frames from a line port 645 to a port that interface with shelf switch);

second base rack (see FIG. 4, a second shelf within a bay 400; also see FIG. 2-3; group 310 (N); see col. 8, line 10; col. 12, line 44-59) including a second line card (see FIG. 4, line card, LC 410 in the second shelf; also see FIG. 3, line card 220 (1,N)) including an egress port, the second line card being capable of processing the packet and further capable of sending the packet to the egress port, the egress port being capable of transmitting the packet (see FIG. 2-3, a port in Line Card 220; also see FIG. 5, Optical transmitter 511 port; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH);

a second switch card (see FIG. 4, Group Matrix SM 420 (N); also see FIG. 2-3, Group Matrix 212 (N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67) including a second cascade port (see FIG. 2-3, a SM 212 (N) port that interface with shelf switch or switching matrix) coupled to the first cascade port, the second switch card being capable of receiving the packet from the first cascade port via the second cascade port (see FIG. 2-3, a SM 212 (N) port and SM 212 (1) are coupled and communicate via shelf switch or switching matrix (i.e. inter shelves communication); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44), the second switch card being in communication with the second line card and capable of routing the packet thereto (see FIG. 4, SM and LC communicates via backplane; see col. 13, line 19-26).

Regarding Claim 35, Zadikian discloses wherein the ingress and egress ports are bi directional (see FIG. 5, bidirectional input/output ports; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32).

Regarding Claim 51, Zadikian discloses a method for switching a packet (see FIG. 1, Router 100; or also see FIG. 3, Router 300 and FIG. 4, Router 400) comprising:

introducing a packet (see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH) into a first port (see FIG. 2, a port in Line Card 220; also see FIG. 5, Optical Receiver 506 and transmitter 511 port) of a first line card (see FIG. 4, line card, LC 410 in the first shelf; also see FIG. 3, line card 220 (1,1)) of a first base rack (see FIG. 4, a first shelf within a bay 400; also see FIG. 3; group 310 (1); see col. 8, line 10; col. 12, line 44-59);

transmitting the packet from the first line card through a first backplane (see FIG. 4, a backplane of the first shelf; see col. 13, line 19-26) to a first switch card of the first base rack (see FIG. 4, Group Matrix SM 420 (1); also see FIG. 2-3, Group Matrix 212 (1-N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67; see FIG. 4, SM communicates and accepts packets/cells/frames via backplane to/from LC; see col. 13, line 19-26);

transmitting the packet from the first switch card to a second switch card (see FIG. 4, Group Matrix SM 420 (N); also see FIG. 2-3, Group Matrix 212 (N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67; also see FIG. 2-3, a SM 212 (N) port and SM 212 (1) are coupled and communicate via shelf switch or switching matrix (i.e. inter shelves communication); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44)) of a second

base rack (see FIG. 4, a second shelf within a bay 400; also see FIG. 2-3; group 310 (N); see col. 8, line 10; col. 12, line 44-59);

transmitting the packet from the second switch card through a second backplane (see FIG. 4, a backplane of the second shelf; see col. 13, line 19-26) to a second line card on the second base rack (see FIG. 4, line card, LC 410 in the second shelf; also see FIG. 3, line card 220 (1,N)); and

transmitting the packet out of a second port of the second base rack (see FIG. 2, a port in Line Card 220; also see FIG. 5, Optical Receiver 506 and transmitter 511 port; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH).

Regarding Claim 52, Zadikian discloses wherein transmitting the packet from the first switch card to the second switch card includes reading a second port number (see FIG. 3-4, LC 410 port number/identification of the second shelf) and determining the second port number is associated with the second base rack (see col. 9, line 25-60; note that in order to route the packets/cells/frames between shelves, the system must identify/read the port number/identification associated with each shelf).

Regarding Claim 53, Zadikian discloses transmitting the packet from a first cascade port on the first switch card (FIG. 2-3, a SM 212 (1) port that interface with shelf switch or switching matrix; also see FIG. 6; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44) to a second cascade port on the second switch card (see FIG. 2-3, a SM 212 (N) port that interface with shelf switch or switching matrix; see FIG. 2-3, a SM 212 (N) port and SM 212 (1) are

coupled and communicate via shelf switch or switching matrix (i.e. inter shelves communication); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44).

Regarding Claim 54, Zadikian discloses transmitting the packet across a connector (see FIG. 2-3, shelf switch or switching matrix) joining the first and second cascade ports (see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44).

Regarding Claims 57 and 74, Zadikian discloses converting the packet from an optical signal to an electrical signal and electrical to optical signal (see col. 13, line 49-69; the line card converts from optical-to-electrical (O/E) at the receiver and electrical-to-optical (E/O) at the transmitter).

Regarding Claims 58 and 73, Zadikian disclose performing a physical layer conversion (see FIG. 5, protocol processor 250 performs a physical layer conversion tasks such as O/E, E/O, clock recovery, mux/demux, etc.; see col. 13, line 49 to col. 14, line 10).

Regarding Claim 71, Zadikian disclose processing the packet by the second line card (see FIG. 5, a combined system of protocol processor 520 and memory 560; see col. 13, line 49 to col. 14, line 9; also perform O/E to E/O conversion; see col. 13, line 49-69).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-9, 16-19,26-29 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of well established teaching in art.

Regarding Claims 2,16 and 26, Zadikian discloses wherein each base rack/shelf includes 12 line cards (see FIG. 4, twelve LC 410) and 3 switch cards (see FIG. 4, three SM 420), and wherein each line card includes 4 ingress/egress ports (see FIG. 5, Transmitter 511,510 and receivers 506 and 505; see col. see col. 13, line 49-61). Zadikian also discloses n line cards, n switch cards, and wherein each line card includes n ports (see FIG. 2-3).

Zadikian does not explicitly disclose 16 line cards, and 4 switch cards, and wherein each line card includes 16 ports. However, it is well know in the art that the switching element comprises 16 line cards, and 4 switch cards, and wherein each line card includes 16 ingress/egress ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide four additional LC cards, 1 additional SM cards, and 12 additional ports, by equating n=16,4 and 16, respectively, as taught by well established teaching in art and Zadikian, so that it would accommodate increasing bandwidth requirement; see Zadikian col. 5, line 19-29, and also it would provide port capacity growth, distributed bandwidth management, and efficient and fast restoration; see Zadikian col. 7, line 15-43.

Regarding Claims 3, 5, 7, 9, 17, 19,27 and 29, Zadikian discloses wherein each switch card of each base rack is in communication with each switch card of each other base rack (see FIG. 2-3, each SM 212 (1 to N) and SM 212 (1 to N) card in each shelf are coupled and communicate via shelf switch or switching matrix (i.e. inter shelves communication); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44).

Regarding Claim 4, Zadikian discloses four base racks (see FIG. 4, four shelves), wherein each base rack/shelf includes 12 line cards (see FIG. 4, twelve LC 410) and 3 switch cards (see FIG. 4, three SM 420), and wherein each line card includes 4 ports (see FIG. 5, Transmitter 511,510 and receivers 506 and 505; see col. see col. 13, line 49-61). Zadikian also discloses n line cards, n switch cards, and wherein each line card includes n ports (see FIG. 2-3).

Zadikian does not explicitly disclose 16 line cards, and 4 switch cards, and wherein each line card includes 16 ports. However, it is well know in the art that the switching element comprises 16 line cards, and 4 switch cards, and wherein each line card includes 16 ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide four additional LC cards, 1 additional SM cards, and 12 additional ports, by equating n=16,4 and 16, respectively, as taught by well established teaching in art and Zadikian, so that it would accommodate increasing bandwidth requirement; see Zadikian col. 5, line 19-29, and also it would provide port capacity growth, distributed bandwidth management, and efficient and fast restoration; see Zadikian col. 7, line 15-43.

Regarding Claim 6 and 18, Zadikian discloses wherein each base rack/shelf includes 4 line cards (see FIG. 4, four LC 410) and 2 switch cards (see FIG. 4, two SM 420), and wherein each line card includes 4 ports (see FIG. 5, Transmitter 511,510 and receivers 506 and 505; see col. see col. 13, line 49-61). Zadikian also discloses n line cards, n switch cards, and wherein each line card includes n ports (see FIG. 2-3).

Zadikian does not explicitly disclose each line card includes 16 ports. However, it is well know in the art that the switching element comprises wherein each line card includes 16 ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to provide 12 additional ports, by equating n= 16, respectively, as taught by well established teaching in art and Zadikian, so that it would accommodate increasing bandwidth requirement; see Zadikian col. 5, line 19-29, and also it would provide port capacity growth, distributed bandwidth management, and efficient and fast restoration; see Zadikian col. 7, line 15-43.

Regarding Claim 8, Zadikian discloses four base racks (see FIG. 4, four shelves), wherein each base rack/shelf includes 4 line cards (see FIG. 4, four LC 410) and 2 switch cards (see FIG. 4, two SM 420), and wherein each line card includes 4 ports (see FIG. 5, Transmitter 511,510 and receivers 506 and 505; see col. see col. 13, line 49-61). Zadikian also discloses n line cards, n switch cards, and wherein each line card includes n ports (see FIG. 2-3).

Zadikian does not explicitly disclose each line card includes 16 ports. However, it is well know in the art that the switching element comprises wherein each line card includes 16 ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 12 additional ports, by equating n= 16, respectively, as taught by well established teaching in art and Zadikian, so that it would accommodate increasing bandwidth requirement; see Zadikian col. 5, line 19-29, and also it would provide port capacity growth, distributed bandwidth management, and efficient and fast restoration; see Zadikian col. 7, line 15-43.

Regarding Claim 28, Zadikian discloses wherein each base rack/shelf includes 4 line cards (see FIG. 4, four LC 410) and 2 switch cards (see FIG. 4, two SM 420), and wherein each line card of the first base rack includes 2 ingress ports (see FIG. 5, receivers 505 and 506; see col. see col. 13, line 49-61), and each line card of the second base rack includes 2 egress ports

(see FIG. 5, transmitters 510 and 511; see col. see col. 13, line 49-61). Zadikian also discloses n line cards, n switch cards, and wherein each line card includes n ports (see FIG. 2-3).

Zadikian does not explicitly disclose each line card includes 16 ingress and 16 egress ports. However, it is well know in the art that the switching element comprises wherein each line card includes 16 ingress and 16 egress ports. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 14 additional ports, by equating n= 16, respectively, as taught by well established teaching in art and Zadikian, so that it would accommodate increasing bandwidth requirement; see Zadikian col. 5, line 19-29, and also it would provide port capacity growth, distributed bandwidth management, and efficient and fast restoration; see Zadikian col. 7, line 15-43.

Regarding Claim 60, Zadikian discloses path packet processing. Zadikian does not explicitly disclose slow-path packet processing. However, it is well know in the art that slowing down or minimizing processing of packet in order to reduce the CPU/processing resources or simply slowing down the path processing of packet in order to control congestion. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide slowing down the path packet processing, as taught by well established teaching in art and Zadikian, so that it would provide efficient and fast restoration; see Zadikian col. 7, line 15-43; and it would also provide to reduce the CPU/processing resources or to control congestion.

7. Claim 10, 11, 20,21,30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Boucher (US006427173B1).

Regarding Claim 10, Zadikian discloses wherein each line card further includes a PHY interface (see FIG. 5, interface of Optical receiver 510 and transmitter 505) and a packet processing (see FIG. 5, a combined system of protocol processor 520 and memory 560) connected in series between the at least one port and the backplane (see FIG. 5, connects between Optical receiver 510 and transmitter 505 port and backplane via optical transmitter 511 and receiver 506); see col. 13, line 49 to col. 14, line 9).

Zadikian does not explicitly disclose a PHY Chip and ASIC. However, Boucher teaches wherein a line card (see FIG. 21, network interface card, INIC 200) further includes a PHY chip (see FIG. 21, PHY chip 2100) and a packet processing ASIC (see FIG. 21, a combined system SRAM 440 and SRAM CTRL 442); see col. 24, line 60 to col. 25, line 16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a PHY chip and ASIC, as taught by Boucher in the system of Zadikian, so that it would greatly increases the speed of that processing and efficiency of transferring data being communicated; see Boucher col. 4, line 14-19.

Regarding Claims 11, 21 and 31, Zadikian discloses a network processor unit (see FIG. 5, CPU 570).

Zadikian does not explicitly disclose ASIC is an SRAM and a DRAM. However, Boucher teaches a packet processing ASIC is a SRAM (see FIG. 21, a combined system SRAM 440 and SRAM CTRL 442, and a network processor unit (see FIG. 21, a combined system of Processor 470, Queue manager 103 and sequencers 2102) coupled to a DRAM (see FIG. 21, DRAM 460); see col. 24, line 60 to col. 25, line 16. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a SRAM and

DRAM, as taught by Boucher in the system of Zadikian, so that it would greatly increases the speed of that processing and efficiency of transferring data being communicated; see Boucher col. 4, line 14-19.

Regarding Claim 20 and 30, Zadikian discloses wherein the first line card of the first base rack (see FIG. 4, line card, LC 410 in the first shelf; also see FIG. 3, line card 220 (1,1)) further includes a first PHY interface (see FIG. 5, interface of Optical receiver 510 and transmitter 505) and a first packet processing (see FIG. 5, a combined system of protocol processor 520 and memory 560) connected in series between the at least one port and the first backplane (see FIG. 5, connects between Optical receiver 510 and transmitter 505 port and backplane via optical transmitter 511 and receiver 506); see col. 13, line 49 to col. 14, line 9); and

wherein the second line card of the second base rack (see FIG. 4, line card, LC 410 in the second shelf; also see FIG. 3, line card 220 (1,N)) further includes a second PHY interface (see FIG. 5, interface of Optical receiver 510 and transmitter 505) and a second packet processing (see FIG. 5, a combined system of protocol processor 520 and memory 560) connected in series between the at least one port and the second backplane (see FIG. 5, connects between Optical receiver 510 and transmitter 505 port and backplane via optical transmitter 511 and receiver 506); see col. 13, line 49 to col. 14, line 9).

Zadikian does not explicitly disclose a PHY Chip and ASIC. However, Boucher teaches wherein a line card (see FIG. 21, network interface card, INIC 200) further includes a PHY chip (see FIG. 21, PHY chip 2100) and a packet processing ASIC (see FIG. 21, a combined system SRAM 440 and SRAM CTRL 442); see col. 24, line 60 to col. 25, line 16). Therefore, it would

have been obvious to one having ordinary skill in the art at the time the invention was made to provide a PHY chip and ASIC, as taught by Boucher in the system of Zadikian, so that it would greatly increases the speed of that processing and efficiency of transferring data being communicated; see Boucher col. 4, line 14-19.

8. Claims 12-14, 22-24, and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Berman (US006904053B1).

Regarding Claim 12, Zadikian discloses wherein each switch card further includes a flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620) coupled to backplane (see FIG. 6, signals towards the backplane; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64).

Zadikian does not explicitly disclose ASIC. However, Berman teaches a control ASIC (see FIG. 29, HUB ASIC); see col. 24, line 5-19. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a ASIC as a control mechanism, as taught by Berman in the system of Zadikian, so that it would reduce the size of the switch; also it would also permit real time routing at gigahertz frequencies; see Berman col. 3, line 30-34 and col. 24, line 14-16.

Regarding Claim 13, Zadikian discloses where the flow control (see FIG. 5, Protocol processor 520) is further coupled to a cascade port (FIG. 2-3, a SM 212 (1) port that interface with shelf switch or switching matrix; see FIG. 6; a port that couples to backplane; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64).

Zadikian does not explicitly disclose a GBIC. However, Berman teaches a control ASIC (see FIG. 29, HUB ASIC) is further coupled to a GBIC; see col. 24, line 5-19. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a GBIC, as taught by Berman in the system of Zadikian, so that it would reduce the size of the switch; also it would also permit real time routing at gigahertz frequencies; see Berman col. 3, line 30-34 and col. 24, line 14-16.

Regarding Claim 14, Zadikian discloses a flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620) coupled to the backplane with four input/output links (see FIG. 6, I/O ports 645(1)-(N); see col. 14, line 49-64).

Zadikian does not explicitly disclose ASIC. Berman teaches a control ASIC (see FIG. 29, HUB ASIC); see col. 24, line 5-19. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a ASIC as a control mechanism, as taught by Berman in the system of Zadikian, so that it would reduce the size of the switch; also it would also permit real time routing at gigahertz frequencies; see Berman col. 3, line 30-34 and col. 24, line 14-16.

Regarding Claims 22 and 32, Zadikian discloses wherein the first switch card (see FIG. 4, Group Matrix SM 420 (1); also see FIG. 2-3, Group Matrix 212 (1-N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67) further includes a first flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620) coupled to a first backplane (see FIG. 6, signals towards the backplane; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64);

wherein the second switch card (see FIG. 4, Group Matrix SM 420 (N); also see FIG. 2-3, Group Matrix 212 (N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67) further includes a first flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620) coupled to a second backplane (see FIG. 6, signals towards the backplane; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64).

Zadikian does not explicitly disclose ASIC. However, Berman teaches a control ASIC (see FIG. 29, HUB ASIC); see col. 24, line 5-19. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a ASIC as a control mechanism, as taught by Berman in the system of Zadikian, so that it would reduce the size of the switch; also it would also permit real time routing at gigahertz frequencies; see Berman col. 3, line 30-34 and col. 24, line 14-16.

Regarding Claims 23 and 33, Zadikian discloses wherein the first switch card further includes where the first flow control (see FIG. 5, Protocol processor 520) is further coupled to a first cascade port ((FIG. 2-3, a SM 212 (1) port that interface with shelf switch or switching matrix; see FIG. 6; a port that couples to backplane; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64); and

wherein the second switch card further includes where the second flow control (see FIG. 5, Protocol processor 520) is further coupled to a second cascade port (FIG. 2-3, a SM 212 (N) port that interface with shelf switch or switching matrix; see FIG. 6; a port that couples to backplane; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64).

Zadikian does not explicitly disclose a GBIC. However, Berman teaches a control ASIC (see FIG. 29, HUB ASIC) is further coupled to a GBIC; see col. 24, line 5-19. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a GBIC, as taught by Berman in the system of Zadikian, so that it would reduce the size of the switch; also it would also permit real time routing at gigahertz frequencies; see Berman col. 3, line 30-34 and col. 24, line 14-16.

Regarding Claims 24 and 34, Zadikian discloses wherein the first flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620 in FIG. 4, Group Matrix SM 420 (1); also see FIG. 2-3, Group Matrix 212 (1)) coupled to the first backplane with four input/output links (see FIG. 6, I/O ports 645(1)-(N); see col. 14, line 49-64); and

a second flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620 in FIG. 4, Group Matrix SM 420 (N); also see FIG. 2-3, Group Matrix 212 (N);) coupled to the first backplane with four input/output links (see FIG. 6, I/O ports 645(1)-(N); see col. 14, line 49-64).

Zadikian does not explicitly disclose ASIC. Berman teaches a control ASIC (see FIG. 29, HUB ASIC); see col. 24, line 5-19. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a ASIC as a control mechanism, as taught by Berman in the system of Zadikian, so that it would reduce the size of the switch; also it would also permit real time routing at gigahertz frequencies; see Berman col. 3, line 30-34 and col. 24, line 14-16.

9. Claims 36,59,61-63, and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Sindhu (US005905725A).

Regarding Claim 36, Zadikian discloses wherein the capability of processing the packet in the first line card includes converting the packet from an optical signal to an electrical signal, and wherein the capability processing the packet in the second line card includes converting the packet from an electrical signal to an optical signal (see col. 13, line 49-69; the line card converts from optical-to-electrical (O/E) at the receiver and electrical-to-optical (E/O) at the transmitter).

Zadikian does not explicitly disclose segmenting the packet to one or more cells and reassembling the one or more cells back to the packet. However, Sindhu teaches wherein the capability of processing the packet in the line card (see FIG. 2B, Input port 107) includes segmenting the packet to one or more cells (see FIG. 3, data handler 304; see col. 4, line 52-65; data handler divides the packet into fixed length cells), and wherein the capability processing the packet in the line card (see FIG. 2B, Output port 108) includes reassembling the one or more cells back to the packet (see FIG. 17, Output formatter 1714; see col. 11, line 50 to col. 12, line 6; coupling the cells back to a packet form). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide dividing and coupling of packets into the cells, as taught by Sindhu in the system of Zadikian, so that it would provide the router with switching the packets at line rates by utilizing the switch architecture that efficiency manages and routes packets through the switch; see Sindhu col. 2, line 65-69.

Regarding Claim 59, Zadikian discloses path packet processing as described above in claim 57-58. Zadikian does not explicitly disclose fast-path packet processing. However, Sindhu teaches fast-path packet processing (see FIG. 2B, Input port 107; see FIG. 3, data handler 304;

see col. 4, line 52-65; data handler divides the packet into fixed length cells in order to perform fast-path packet processing). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide dividing packets into the cells to provide fast-path packet processing, as taught by Sindhu in the system of Zadikian, so that it would provide the fast router with switching the packets at line rates by utilizing the switch architecture that efficiency manages and routes packets through the switch; see Sindhu col. 2, line 65-69.

Regarding Claim 61, Zadikian does not explicitly disclose segmenting the packet into at least one cell. However, Sindhu teaches segmenting the packet into at least one cell (see FIG. 3, data handler 304; see col. 4, line 52-65; data handler divides the packet into fixed length cells). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide dividing of packets into the cells, as taught by Sindhu in the system of Zadikian, for the same motivation as described above in claim 36.

Regarding Claim 62, Sindhu discloses wherein segmenting the packet creates a payload of 128 bytes (see FIG. 4b; see col. 4, line 55-61; 64 bytes of cell data). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 64 bytes of cell data, as taught by Sindhu in the system of Zadikian, for the same motivation as described above in claim 36.

Regarding Claim 63, Sindhu discloses wherein segmenting the packet creates a payload of 128 bytes (see FIG. 4b; see col. 4, line 55-61; 64 bytes of cell data). Neither Zadikian nor Sindhu explicitly discloses 128 bytes. However, setting cell data/payload length to 128 bytes (i.e. 2 time more than Sindhu's 64 bytes) does not define a patentable distinct invention over that in the combined system of Zadikian and Sindhu since both the invention as a whole and the

combined system of Zadikian and Sindhu are directed to determining the length of cell/payload data. The degree in which determining length of segmenting cell presents no new or unexpected results, so long as the cells are segmented, the traffic is processed in a successful way. Therefore, to have a segmented cell size to 128 bytes would have been routine experimentation and optimization in the absence of criticality.

Regarding Claim 72, Zadikian does not explicitly disclose reassembling at least one cell into the packet. However, Sindhu teaches reassembling the one or more cells back to the packet (see FIG. 17, Output formatter 1714; see col. 11, line 50 to col. 12, line 6; coupling the cells back to a packet form). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide coupling of packets into the cells, as taught by Sindhu in the system of Zadikian, so that it would provide the router with switching the packets at line rates by utilizing the switch architecture that efficiency manages and routes packets through the switch; see Sindhu col. 2, line 65-69.

10. Claims 37, 48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Wilkins (US 20050050240A1).

Regarding Claim 37, Zadikian discloses a switching device (see FIG. 1, Router 100; or also see FIG. 3, Router 300 and FIG. 4, Router 400) comprising:

a first base rack (see FIG. 4, a first shelf within a bay 400; also see FIG. 3; group 310 (1); see col. 8, line 10; col. 12, line 44-59) including a first line card (see FIG. 4, line card, LC 410 in the first shelf; also see FIG. 3, line card 220 (1,1)) having an ingress port capable of receiving a packet (see FIG. 2, a port in Line Card 220; also see FIG. 5, Optical Receiver 506; see col. 4, line

54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH), the first line card being capable of processing the packet (see FIG. 5, Protocol processor 520, CPU 570, Transceiver 580,transformer 585,switch 590; see col. 13, line 39 to col. 14, line 43);

a first switch card (see FIG. 4, Group Matrix SM 420 (1); also see FIG. 2-3, Group Matrix 212 (1-N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67) in communication with the first line card and capable of accepting the packet therefrom (see FIG. 4, communicates and accepts packets/cells/frames via backplane; see col. 13, line 19-26), the first switch card including a first cascade port (FIG. 2-3, a SM 212 (1) port that interface with shelf switch or switching matrix), the first switch card capable of routing the packet to the first cascade port (see FIG. 6; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; a group matrix card routes/forwards packets/cells/frames from a line port 645 to a port that interface with shelf switch);

second base rack (see FIG. 4, a second shelf within a bay 400; also see FIG. 2-3; group 310 (N); see col. 8, line 10; col. 12, line 44-59) including a second line card (see FIG. 4, line card, LC 410 in the second shelf; also see FIG. 3, line card 220 (1,N)) including an egress port, the second line card being capable of processing the packet and further capable of sending the packet to the egress port, the egress port being capable of transmitting the packet (see FIG. 2-3, a port in Line Card 220; also see FIG. 5, Optical transmitter 511 port; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32; note that wideband and broadband ATM, frame relay, FDDI, HDLC packets/cells are carried within SONET/SDH);

a second switch card (see FIG. 4, Group Matrix SM 420 (N); also see FIG. 2-3, Group Matrix 212 (N); see FIG. 6, a group matrix 600); see col. 9, line 26-41; see col. 12, line 46-67) including a second cascade port (see FIG. 2-3, a SM 212 (N) port that interface with shelf switch or switching matrix) coupled to the first cascade port, the second switch card being capable of receiving the packet from the first cascade port via the second cascade port (see FIG. 2-3, a SM 212 (N) port and SM 212 (1) are coupled and communicate via shelf switch or switching matrix (i.e. inter shelves communication); see col. 9, line 25-41, 60 to col. 10, line 10; see col. 11, line 24-44), the second switch card being in communication with the second line card and capable of routing the packet thereto (see FIG. 4, SM and LC communicates via backplane; see col. 13, line 19-26).

Zadikian does not explicitly disclose a storage device coupled and a server. However, Wilkins teaches a storage device (see FIG. 1, Disk 103 from Disk array 102) coupled to the ingress port (see FIG. 1, I/O ports of Fibre channel switch 111); and

a server (see FIG. 1, Server 108 from Server Array 112) coupled to the egress port (see FIG. 1, I/O ports of Fibre channel switch 111); see page 2, paragraph 26-27. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to switch between server and storage/disk, as taught by Wilkins in the system of Zadikian, so that it would provide switching capability between servers to disks; see Wilkins page 2, paragraph 27; and it would also increase throughput; see Wilkins page 5, paragraph 48.

Regarding Claim 48, Wilkins discloses the storage device includes RAID (see page 2, paragraph 25-26). Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to provide a RAID, as taught by Wilkins and Zadikian, in the system of Zadikian for the same motivation as stated in claim 37.

Regarding Claim 50, Wilkins discloses the storage device includes tape backup (see FIG. 1, disk array 102; see page 2, paragraph 25-26; a disk array comprises disks 103 for storage for backup). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a tape storage for backup, as taught by Wilkins and Zadikian, in the system of Zadikian for the same motivation as stated in claim 37.

11. Claims 38-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Wilkins as applied to claim 37 above, and further in view of well established teaching in art.

Regarding Claim 38, a claim substantially discloses all the limitations of the respective claim 26 above. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide four additional LC cards, 1 additional SM cards, and 12 additional ports, by equating n=16,4 and 16, respectively, as taught by well established teaching in art and Zadikian, in the combined system of Zadikian and Wilkins for the same motivation as stated in claim 26.

Regarding Claims 39 and 41, a claim substantially discloses all the limitations of the respective claim 3, 5, 7, 9, 17, 19,27 and 29 above. Therefore, they are subject to the same rejection.

Regarding Claim 40, a claim substantially discloses all the limitations of the respective claim 28 above. Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to provide 14 additional ports, by equating n= 16, respectively, as taught by well established teaching in art and Zadikian, in the combined system of Zadikian and Wilkins for the same motivation as stated in claim 28.

Regarding Claim 42, a claim substantially discloses all the limitations of the respective **claim 30** above. Therefore, it is subject to the same rejection.

Regarding Claim 43, a claim substantially discloses all the limitations of the respective **claim 31** above. Therefore, it is subject to the same rejection.

Regarding Claim 44, a claim substantially discloses all the limitations of the respective **claim 32** above. Therefore, it is subject to the same rejection.

Regarding Claim 45, a claim substantially discloses all the limitations of the respective **claim 33** above. Therefore, it is subject to the same rejection.

Regarding Claim 46, a claim substantially discloses all the limitations of the respective **claim 34** above. Therefore, it is subject to the same rejection.

12. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Wilkins as applied to claim 37 above, and further in view of Sheets (US 20050182838A1).

Regarding Claim 47, Wilkins discloses the system network comprises an IP switch (see FIG. 1, Ethernet Hub/Switch 106; see page 2, paragraph 27). Neither Zadikian nor Wilkins explicitly discloses IP router. However, Sheets discloses the system area network comprises an IP router (see FIG. 1, Network Router 26) and an IP switch (see FIG. 1, Network switches 24); see page 1, paragraph 39).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide IP router, as taught by Sheets, in the combined system of Zadikian and Wilkins, so that it would provide a hosted service provide for the Internet is such a way to provide dynamic management of hosted services across disparate customer and also provide flexible server farm arrangement; see Sheets page 3, paragraph 19 and page4, paragraph 21.

13. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Wilkins as applied to claim 37 above, and further in view of Lieber (US006658504B1).

Regarding Claim 49, Neither Zadikian nor Wilkins explicitly discloses JBOD. However, Sheets discloses the storage device comprises JBOD (see col. 3, line 5-9; see col. 7, line 1-5; JBOD).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide JBOD, as taught by Lieber, in the combined system of Zadikian and Wilkins, so that it would provide function of the JBOD as SAN without requiring any mechanical or electrical changes; see Lieber col. 3, line 5-10.

14. Claims 67,68,77 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Oliva (US006504820B1).

Regarding Claim 67, Zadikian discloses wherein transmitting the packet through the second backplane includes placing the packet on the second switch card as described above in claim 51.

Zadikian does not explicitly disclose placing a packet in a priority output queue. However, Oliva teaches placing a packet in a priority output queue (see FIG. 2A, placing cells/packets in priority output queues VPs 58; see FIG. 2B, placing cell/packets in priority output queue VC 74; see col. 5, line 55 to col. 6, line 12; see col. 7, line 6-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide placing a packet in a priority output queue, as taught by Oliva in the system of Zadikian, so that it would more efficiently utilize bandwidth based on measurements that may be more accurate and efficient; see Oliva col. 2, line 55-60.

Regarding Claim 68, Zadikian discloses wherein transmitting the packet through the second backplane to use the second port as described above in claim 51.

Zadikian does not explicitly disclose scheduling. However, Oliva teaches wherein transmitting the packet further includes scheduling to use the port (see FIG. 2A, Server 60; see FIG. 2b, server 76; server utilizes scheduling the switch port; see col. 6, line 30 to col. 7, line 20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide scheduling, as taught by Oliva in the system of Zadikian, for the same motivation as described above in claim 67.

Regarding Claim 77, Zadikian discloses routing the packet through a crossbar (see FIG. 6, a cross connection/bar between Selector 610 and broadcasts units 620) on the first switch card and dedicated to a cascade port on the first base rack (FIG. 2-3, a SM 212 (1) port that interface with shelf switch or switching matrix; see FIG. 6; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; a group matrix card routes/forwards packets/cells/frames from a line port 645 to a port that interface with shelf switch).

Zadikian does not explicitly disclose buffering the packet in a first queue. However, Oliva teaches buffering a packet in a first queue (see FIG. 2A, placing cells/packets in priority output queues VPs 58; see FIG. 2B, buffering cell/packets in queue VC 74; see col. 5, line 55 to col. 6, line 12; see col. 7, line 6-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide buffering a packet in a queue, as taught by Oliva in the system of Zadikian, so that it would more efficiently utilize bandwidth based on measurements that may be more accurate and efficient; see Oliva col. 2, line 55-60.

Regarding Claim 79, Zadikian discloses routing the packet through a crossbar on the second switch card (see FIG. 6, a cross connection/bar between Selector 610 and broadcasts units 620) and sending the packet between the crossbar and the second backplane (see FIG. 6; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; a group matrix card routes/forwards packets/cells/frames from a cross connection/bar to a backplane).

Zadikian does not explicitly disclose buffering the packet in a queue. However, Oliva teaches buffering the packet in a queue (see FIG. 2A, placing cells/packets in priority output queues VPs 58; see FIG. 2B, buffering cell/packets in queue VC 74; see col. 5, line 55 to col. 6, line 12; see col. 7, line 6-20) between the crossbar (see FIG. 2A-B, a cross connection to server S 60 or 76) and the backplane (see FIG. 2A-B, a connection/bus 50 or 72); see col. 5, line 55 to col. 6, line 12; see col. 7, line 6-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide buffering a packet in a queue, as taught by Oliva in the system of Zadikian, so that it would more efficiently utilize

bandwidth based on measurements that may be more accurate and efficient; see Oliva col. 2, line 55-60.

15. Claim 75, 76 and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zadikian in view of Khacherian (US006542507B1).

Regarding Claim 75, Zadikian discloses a packet processor on the line card (see FIG. 5, a combined system of protocol processor 520 and memory 560).

Zadikian does not explicitly disclose a set of queues. However, Khacherian teaches buffering the packet in a set of queues (see FIG. 2, input queues 212) on the line card (see FIG. 2, Input card/module 210; see col. 3, line 41-69; also see FIG. 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a set of queues to input card/unit, as taught by Khacherian in the system of Zadikian, so that it would improve buffer control arrangement suitable for a high speed, high performance switch; see Khacherian col. 2, line 44-46.

Regarding Claim 76, Zadikian discloses wherein each switch card further includes a flow control (see FIG. 5, a combined system of microcontroller 630, selector 610 and broadcast unit 620; see col. 9, line 25-41, 60 to col. 10, line 5; see col. 11, line 24-44; see col. 14, line 49-64).

Zadikian does not explicitly disclose a set of queues and ASIC. However, Khacherian teaches buffering the packet in a set of queues (see FIG. 2, input queues 212) on the line card (see FIG. 2, Input card/module 210; see col. 3, line 41-69; also see FIG. 3) and ASIC (see col. 6, line 50-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a set of queues to input card/unit and ASIC for flow

controlling, as taught by Khacherian in the system of Zadikian, so that it would improve buffer control arrangement suitable for a high speed, high performance switch; see Khacherian col. 2, line 44-46.

Regarding Claim 80, Zadikian discloses sending the packet on the second line card dedicated to a destination port (see FIG. 2-3, a port in Line Card 220; also see FIG. 5, Optical transmitter 511 port; see col. 4, line 54-66; col. 9, line 26-35; see col. 13, line 49-61; see col. 8, line 25-32).

Zadikian does not explicitly disclose buffering the packet in a queue. However, Khacherian teaches buffering the packet in a queue (see FIG. 2, input queues 212) on the line card (see FIG. 2, Input card/module 210; see col. 3, line 41-69; also see FIG. 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a queue to input card/unit, as taught by Khacherian in the system of Zadikian, so that it would improve buffer control arrangement suitable for a high speed, high performance switch; see Khacherian col. 2, line 44-46.

Allowable Subject Matter

16. Claims 55,56,64-66,69,70 and 78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM

9/21/05

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600